

WHAT IS CLAIMED IS:

1. An ATM optical signal matching apparatus, comprising:
a plurality of photoelectric conversion parts for photoelectric-converting input
5 data; ^{10a, b}
a plurality of user-network matching parts for processing signals
transmitted/received through the photoelectric conversion parts; ^{12a, b}
a bus switch for exchanging signals with the plurality of user-network
matching parts; ^{16a, 16b}
10 a loop back processor for returning a signal received through the bus switch to
an original transmitter sending the signal according to a predetermine control signal;
and ^{18a, 18b}
a controller for providing a control signal to the user-network matching parts
and the loop back processor according to a program stored therein. ¹⁹
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2. The ATM optical signal matching apparatus as claimed in claim 1,
wherein each of the plurality of photoelectric conversion parts photoelectric-converts
data having the transfer rate of 155.520Mbps.
- 20 3. The ATM optical signal matching apparatus as claimed in claim 1,
wherein each of the plurality of user-network matching parts is connected to four of the
photoelectric conversion parts to match data at the transfer rate of 622Mbps.
4. The ATM optical signal matching apparatus as claimed in claim 1,

wherein the controller includes a flash memory that is a nonvolatile memory, a synchronous RAM that is a volatile memory, and a microprocessor connected to the flash memory and the synchronous RAM to perform a predetermined operation function.

5 5. The ATM optical signal matching apparatus as claimed in claim 1,
further comprising a first oscillator connected to the user-network matching parts to
generate a reference clock for synchronizing data transmitted/received at the transfer
rate of 155.520Mbps, and a second oscillator connected to the user-network matching
parts for generating a predetermined clock as the system clock of the user-network
10 matching parts to match transmission/reception data to UTOPIA level 2

 6. The ATM optical signal matching apparatus as claimed in claim 5,
wherein the first oscillator generates 19.44MHz clock and the second oscillator
generates 50MHz clock.

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